F-Tile CPRI PHY Intel® FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **23.3**

IP Version: **4.3.0**

Online Version
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Contents

1. About the F-Tile CPRI PHY Intel® FPGA IP Core

The F-Tile CPRI PHY Intel® FPGA IP core implements the physical layer (layer 1) specification in the Intel Agilex™ 7 devices based on the *Common Public Radio Interface (CPRI) v7.0 Specification (2015-10-09)*.

Related Information

- F-Tile CPRI PHY Intel FPGA IP Design Example User Guide
- F-Tile CPRI PHY Intel FPGA IP Release Notes

1.1. Supported Features

The F-Tile CPRI PHY Intel FPGA IP core supports the following features:

- Compliant with the *CPRI Specification V7.0 (2015-10-09)*.
- Supports line bit rates of;
  - 1.228 Gbps
  - 2.4576 Gbps
  - 3.072 Gbps
  - 4.9152 Gbps
  - 6.144 Gbps
  - 9.8304 Gbps
  - 10.1376 Gbps with and without RS-FEC
  - 12.1651 Gbps with and without RS-FEC
  - 24.33024 Gbps with and without RS-FEC
- Supports deterministic latency measurement.
- Provides register access interface to external or on-chip processor, using the Intel Avalon® memory-mapped interconnect specification.
- Supports Physical Medium Attachment (PMA) adaptation.

Table 1. Available Features

CPRI Line Bit Rate (Gbps)	RS-FEC Support	Reference Clock (MHz)	Deterministic Latency Support
1.2288	No	153.6 or 122.88	Yes
2.4576	No	153.6 or 122.88	Yes
3.072	No	153.6 or 122.88	Yes
4.9152	No	153.6 or 122.88	Yes

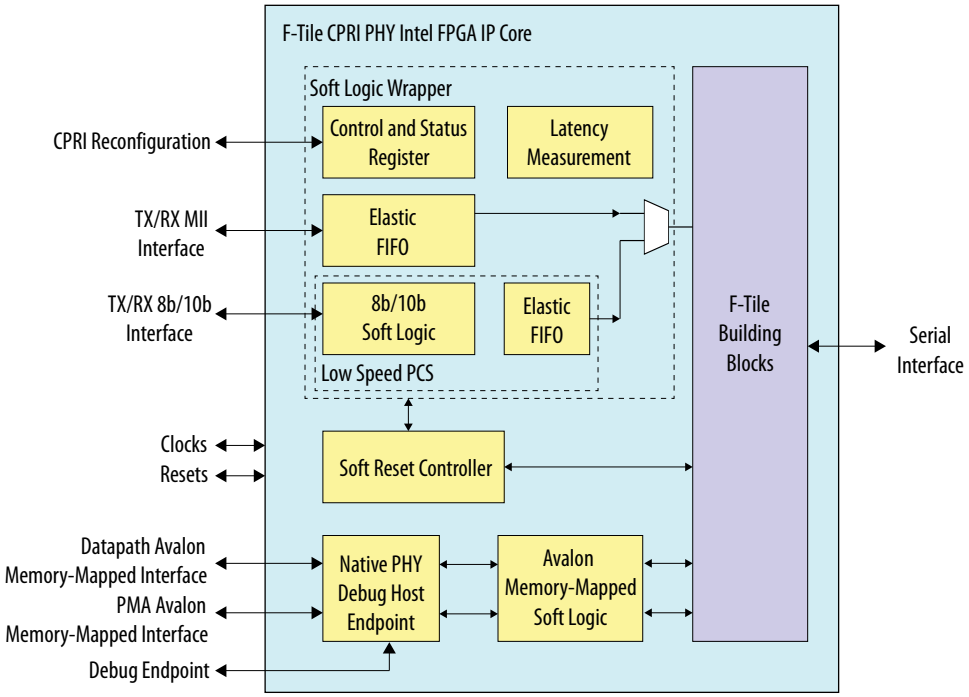
continued...

CPRI Line Bit Rate (Gbps)	RS-FEC Support	Reference Clock (MHz)	Deterministic Latency Support
6.144	No	153.6 or 122.88	Yes
9.8304	No	153.6 or 122.88	Yes
10.1376	With and Without	184.32 or 122.88	Yes
12.1651	With and Without	184.32 or 122.88	Yes
24.33024	With and Without	184.32 or 122.88	Yes

1.2. Overview

The F-Tile CPRI PHY Intel FPGA IP block diagram shows the main blocks, and internal and external connections for each variant.

Figure 1. IP Block Diagram



- The RS-FEC block is optional for the IP core variations that target 10.1376, 12.1651, and 24.33024 Gbps CPRI line rate.
- The soft reset controller implements the reset sequence of the IP core.
- The IP variation with 1.2288, 2.4576, 3.072, 4.9152, 6.144, and 9.8304 Gbps CPRI line rate include 8b/10b soft PCS.
- The IP variations that target CPRI line rates of 10.1376, 12.1651, and 24.33024 Gbps use 64b/66b hard PCS within the F-tile.
- It supports latency measurement for delay calculation between the FPGA pins to the core.

1.3. Device Family Support

Table 2. Intel FPGA IP Core Device Support Levels

Device Support Level	Definition
Advance	The IP core is available for simulation and compilation for this device family. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (datapath width, burst depth, I/O standards tradeoffs).
Preliminary	The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.
Final	The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Table 3. F-Tile CPRI PHY Intel FPGA IP Core Device Family Support

This table shows the level of support for each Intel FPGA device family.

Device Family	Support
Intel Agilex 7 devices (with F-tile)	Advance
Other device families	No support

1.4. Device Speed Grade Support

The F-Tile CPRI PHY Intel FPGA IP core supports Intel Agilex 7 devices with these speed grade properties:

- Transceiver speed grade: -1 or -2
- Core speed grade: -1 or -2 or -3

1.5. Resource Utilization

This section covers the resource utilization for different variations of the F-Tile CPRI PHY Intel FPGA IP core using the Intel Quartus® Prime Pro Edition software version 21.4.

Table 4. Resource Utilization for Intel Agilex 7 Devices

CPRI Line Bit Rate (With number of channel1)	ALMs	ALUTs	Dedicated Logic Registers	Memory 20K
24.33024 Gbps with RS-FEC	8826	13269	9885	12
24 Gbps without RS-FEC	8866	13267	9890	12
12.1651 Gbps with RS-FEC	8856	13267	9890	12
12.1651 Gbps without RS-FEC	8856	13267	9890	12
10.1376 Gbps with RS-FEC	8856	13267	9888	12
10.1376 Gbps without RS-FEC	8856	13267	9888	12

continued...

CPRI Line Bit Rate (With number of channel1)	ALMs	ALUTs	Dedicated Logic Registers	Memory 20K
9.8304 Gbps	9636	13873	10969	12
6.144 Gbps	9667	13875	10957	12
4.9152 Gbps	9664	13878	10965	12
3.072 Gbps	9667	13875	10952	12
2.4576 Gbps	9666	13878	10949	12
1.2288 Gbps	9686	13878	10940	12

1.6. Release Information

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 5. F-Tile CPRI PHY Intel FPGA IP Core Release Information

Item	Description
IP Version	4.3.0
Intel Quartus Prime Version	23.3
Release Date	2023.10.02
Ordering Code	IP-CPRI-v7-E-PHY

2. Getting Started

The following sections explain how to install, parameterize, simulate, and initialize the F-Tile CPRI PHY Intel FPGA IP core.

2.1. Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime Pro Edition software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

Figure 2. IP Core Installation Path

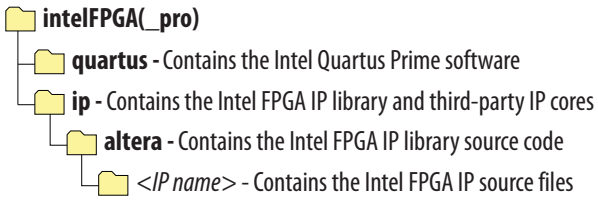


Table 6. IP Core Installation Locations

Location	Software	Platform
`<drive>:\intelFPGA_pro\quartus\ip\altera`	Intel Quartus Prime Pro Edition software	Windows*
`<home directory>:/intelFPGA_pro/quartus/ip/altera`	Intel Quartus Prime Pro Edition software	Linux*

2.1.1. Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

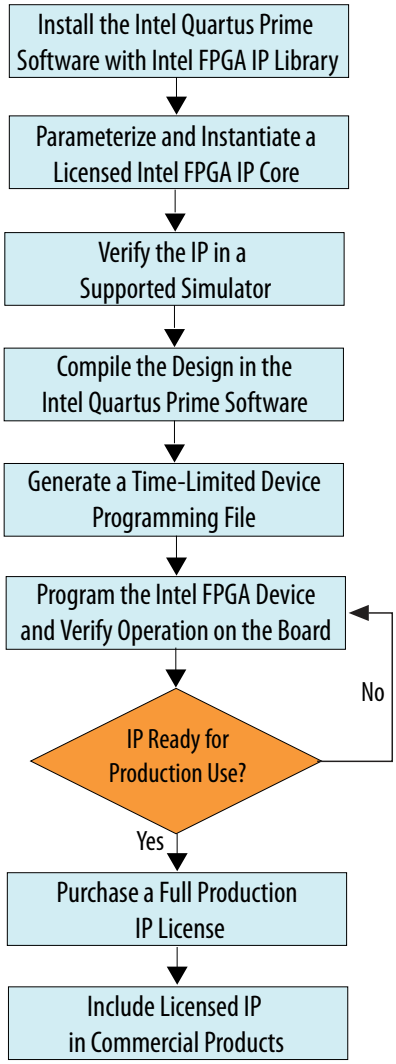
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (*<project name>*`_time_limited.sof`) that expires at the time limit.

Figure 3. Intel FPGA IP Evaluation Mode Flow



Note: Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the Intel FPGA Self-Service Licensing Center.

The Intel FPGA Software License Agreements govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

Related Information

- Intel FPGA Licensing Support Center
- Introduction to Intel FPGA Software Installation and Licensing

2.2. Specifying the IP Core Parameters and Options

The IP parameter editor allows you to quickly configure your custom IP variation. Use the following steps to specify IP core options and parameters in the Intel Quartus Prime Pro Edition software.

1. If you do not already have an Intel Quartus Prime Pro Edition project in which to integrate your F-Tile CPRI PHY Intel FPGA IP core, you must create one.
   a. In the Intel Quartus Prime Pro Edition, click **File ➤ New Project Wizard** to create a new Quartus Prime project, or **File ➤ Open Project** to open an existing Quartus Prime project. The wizard prompts you to specify a device.
   b. Specify the device family Intel Agilex 7 and select a F-tile device that meets the speed grade requirements for the IP core.
   c. Click **Finish**.
2. In the IP Catalog, locate and select **F-Tile CPRI PHY Intel FPGA IP**. The **New IP Variation** window appears.
3. Specify a top-level name for your new custom IP variation. The parameter editor saves the IP variation settings in a file named *<your_ip>*`.ip`.
4. Click **OK**. The parameter editor appears.
5. Specify the parameters for your IP core variation. Refer to IP Parameter Settings on page 15 for information about specific IP core parameters.
6. Optionally, to generate a simulation testbench or compilation and hardware design example, follow the instructions in the *F-Tile CPRI PHY Intel FPGA IP Design Example User Guide*.
7. Click **Generate HDL**. The **Generation** dialog box appears.
8. Specify output file generation options, and then click **Generate**. The IP variation files generate according to your specifications.
9. Click **Finish**. The parameter editor adds the top-level `.ip` file to the current project automatically. If you are prompted to manually add the `.ip` file to the project, click **Project ➤ Add/Remove Files in Project** to add the file.
10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports and set any appropriate per-instance RTL parameters.

Related Information

F-Tile CPRI PHY Intel FPGA IP Design Example User Guide

2.2.1. Reference and System PLL Clock for your IP Design

Each F-tile system must instantiate one F-Tile Reference and System PLL Clocks Intel FPGA IP. The F-Tile Reference and System PLL Clocks Intel FPGA IP performs three main functions:

1. Configure reference clock for FHT PMA:

- Enable the FHT common PLLs and select the reference clock source for FHT common PLL
- Specify the FHT reference clock source frequency

Note: The F-Tile CPRI PHY Intel FPGA IP core does not support FHT PMA. The IP core implementation uses FGT PMA.

2. Configure reference clock for FGT PMA:
   - Enable FGT reference clocks and specify the reference clock frequency
   - Specify FGT CDR output
3. Configure system PLL:
   - Enable system PLL and specify its mode
   - Specify the reference clock source and frequency for system PLL

Note: In your IP design, you must include an F-Tile Reference and System PLL Clocks Intel FPGA IP core to pass logic generation flow.

The F-Tile Reference and System PLL Clocks Intel FPGA IP must always connect to a protocol based Intel FPGA IP. The F-Tile Reference and System PLL Clocks Intel FPGA IP cannot be compiled or simulated as a standalone IP. For more information on parameters and port list for F-Tile Reference and System PLL Clocks Intel FPGA IP core, refer to *Implementing the F-Tile Reference and System PLL Clocks Intel FPGA IP* section of the *F-tile Architecture and PMA and FEC Direct PHY IP User Guide*.

When you design multiple interfaces or protocol-based IP cores within a single F-tile, you must use only one instance of the F-Tile Reference and System PLL Clocks Intel FPGA IP core to configure:

- All required reference clocks for FGT PMA (up to 10) and FHT PMA (up to 2) to implement multiple interfaces within a single F-tile.
- All required FHT common PLLs (up to 2) to implement multiple interfaces within a single F-tile.
- All required System PLLs (up to 3) to implement multiple interfaces within a single F-tile.
- All required reference clocks for system PLLs (up to 8 – shared with FGT PMA) to implement multiple interfaces within a single F-tile.

When you design multiple interfaces or protocol-based IP cores within a single F-tile, you can only use three System PLLs. For example, you can use one System PLL for PCIe and two for Ethernet and other protocols. However, there are other use cases where you can use all three for various interfaces within the Ethernet and PMA-Direct digital blocks. As there are only three System PLLs, multiple interfaces or protocol-based IP cores with different line rates may have to share a System PLL. While sharing a System PLL, the interface with the highest line rate determines the system PLL frequency, and the interfaces with the lower line rates must be overclocked. For more information, refer to *Implementing the F-Tile Reference and System PLL Clocks Intel FPGA IP* section of the *F-tile Architecture and PMA and FEC Direct PHY IP User Guide*.

Related Information

F-tile Architecture and PMA and FEC Direct PHY IP User Guide

2.3. Generated File Structure

The Intel Quartus Prime Pro Edition software generates the following IP core output file structure.

For information about the file structure of the design example, refer to the device specific *F-Tile CPRI PHY Intel FPGA IP Design Example User Guide*.

Figure 4. File Structure

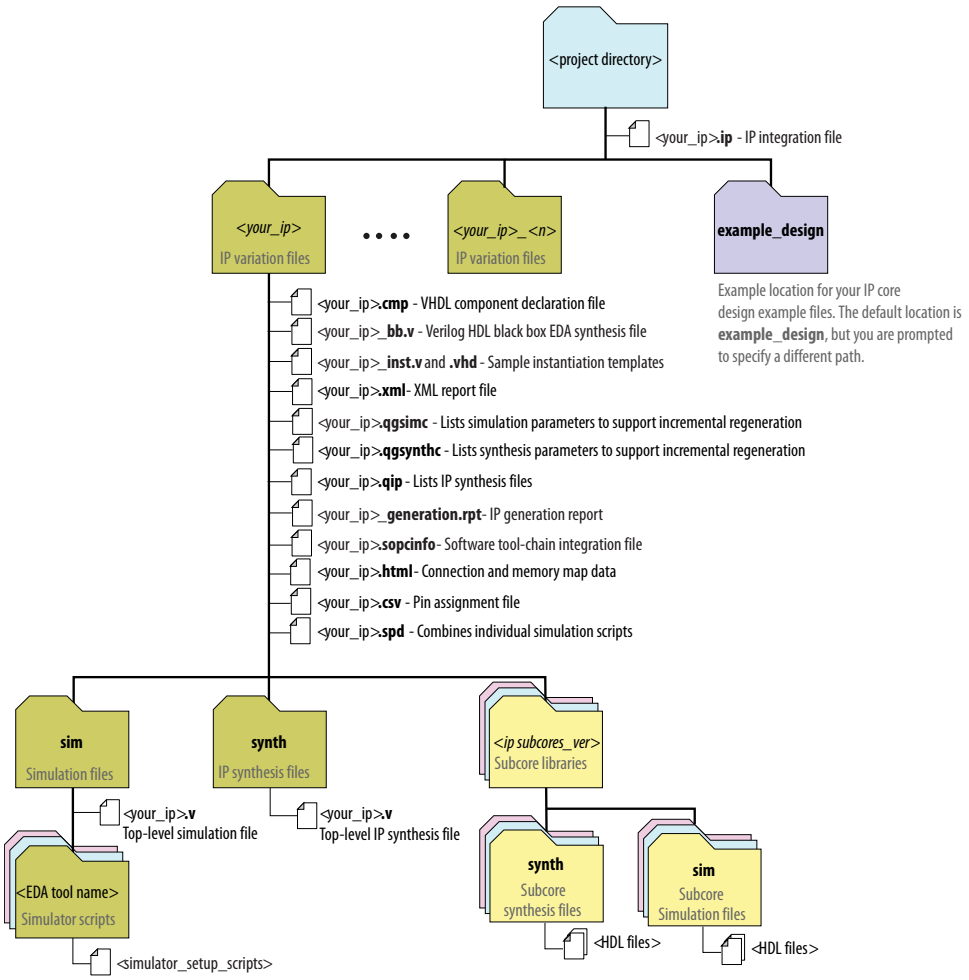


Table 7. Generated Files

File Name	Description
<*your_ip*>.ip	The Platform Designer system or top-level IP variation file. <*your_ip*> is the name that you give your IP variation.
<*your_ip*>.cmp	The VHDL Component Declaration (.cmp) file is a text file that contains local generic and port definitions that you can use in VHDL design files.
<*your_ip*>.html	A report that contains connection information, a memory map showing the address of each agent with respect to each host to which it is connected, and parameter assignments.

continued...

File Name	Description
<*your_ip*>_generation.rpt	IP or Platform Designer generation log file. A summary of the messages during IP generation.
<*your_ip*>.qgsimc	Lists simulation parameters to support incremental regeneration.
<*your_ip*>.qgsynthc	Lists synthesis parameters to support incremental regeneration.
<*your_ip*>.qip	Contains all the required information about the IP component to integrate and compile the IP component in the Intel Quartus Prime software.
<*your_ip*>.sopcinfo	Describes the connections and IP component parameterizations in your Platform Designer system. You can parse its contents to get requirements when you develop software drivers for IP components. Downstream tools such as the Nios® II tool chain use this file. The .sopcinfo file and the system.h file generated for the Nios II tool chain include address map information for each agent relative to each host that accesses the agent. Different hosts may have a different address map to access a particular agent component.
<*your_ip*>.csv	Contains information about the upgrade status of the IP component.
<*your_ip*>.spd	Required input file for ip-make-simscript to generate simulation scripts for supported simulators. The .spd file contains a list of files generated for simulation, along with information about memories that you can initialize.
<*your_ip*>_bb.v	You can use the Verilog black-box (_bb.v) file as an empty module declaration for use as a black box.
<*your_ip*>_inst.v or _inst.vhd	HDL example instantiation template. You can copy and paste the contents of this file into your HDL file to instantiate the IP variation.
<*your_ip*>.v or <*your_ip*>.vhd	HDL files that instantiate each submodule or child IP core for synthesis or simulation.
mentor/	Contains a Siemens* EDA QuestaSim* or Questa* Intel FPGA Edition script msim_setup.tcl to set up and run a simulation.
synopsys/vcs/ synopsys/vcsmx/	Contains a shell script vcs_setup.sh to set up and run a Synopsys* VCS* simulation. Contains a shell script vcsmx_setup.sh and synopsys_ sim.setup file to set up and run a Synopsys VCS MX simulation.
xcelium/	Contains a shell script xcelium_setup.sh to set up and run a Xcelium* simulation.
<*child IP cores*>/	For each generated child IP core directory, Platform Designer generates synth/ and sim/ sub-directories.

Related Information

F-Tile CPRI PHY Intel FPGA IP Design Example User Guide

2.4. IP Core Testbenches

Intel provides a testbench and compilation-only design example that you can generate for the F-Tile CPRI PHY Intel FPGA IP core.

To generate the testbench, in the F-Tile CPRI PHY Intel FPGA IP parameter editor, you must first set the parameter values for the IP core variation you intend to generate in your end product. If you do not set the parameter values for your DUT to match the parameter values in your end product, the testbench you generate does not exercise the IP core variation you intend.

The testbench demonstrates XGMII data transfer to PHY with internal serial loopback and performs basic latency calculations. It is not intended to be a substitute for a full verification environment.

Note: A compilation-only design example provides reports of timing and resource utilization. It is not a hardware testing design example.

Related Information

F-Tile CPRI PHY Intel FPGA IP Design Example User Guide

3. IP Parameter Settings

You customize the IP core by specifying parameters in the IP parameter editor.

Figure 5. IP Parameter Editor

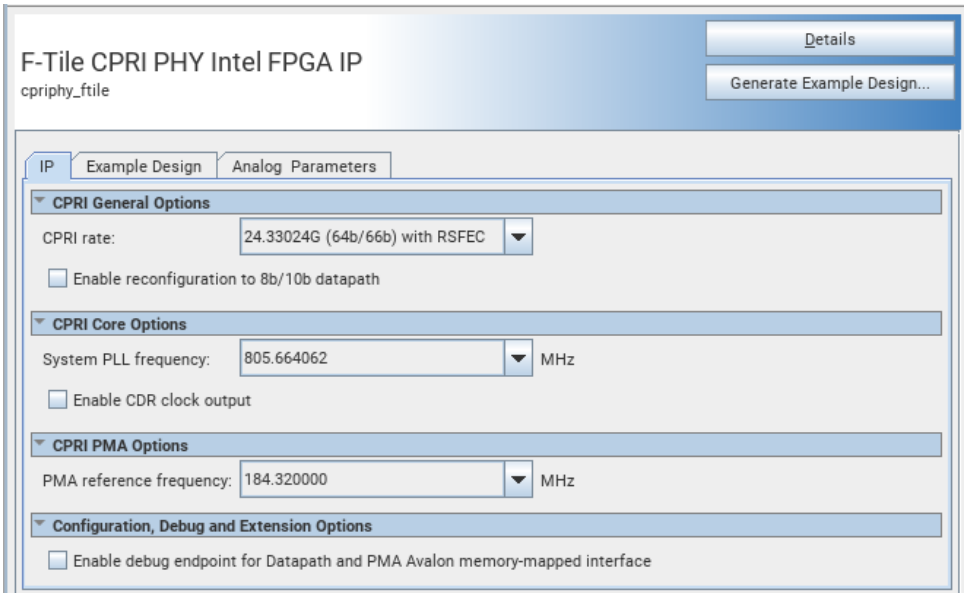


Table 8. Parameter Settings: IP Tab

Parameter	Supported Values	Default Setting	Description
CPRI General Options			
CPRI Rate	• 1.2288G (8b/10b) • 2.4376G (8b/10b) • 3.072G (8b/10b) • 4.9152G (8b/10b) • 6.144G (8b/10b) • 9.8304G (8b/10b) • 10.1376G (64b/66b) • 10.1376G (64b/66b) • 12.16512G (64b/66b) • 12.16512G (64b/66b) with RS-FEC • 24.33024G (64b/66b) • 24.33024G (64b/66b) with RS-FEC	24.33024G (64b/66b) with RS-FEC	Selects the CPRI data rate. The hard RS-FEC block is included in the core if you select 10.1376, 12.1651, and 24.33024 Gbps (64b/66b) with the RS-FEC option.

continued...

Parameter	Supported Values	Default Setting	Description
Enable Reconfiguration to 8b/10b Datapath	• On • Off	Off	Turn on this parameter if you plan to reconfigure the CPRI line rate of your channels from 64b/66b datapath rates to 8b/10b datapath rates at run-time. If this option is not enabled, the CPRI IP core uses fewer resources, and you cannot change to 8b/10b datapath rates at run-time.
CPRI Core Options			
System PLL Frequency	• 805.664062 MHz • 830.078125 MHz • 903.125 MHz	805.664062 MHz	Select the System PLL frequency for your IP.
Enable CDR Clock Output	• On • Off	Off	Turn on this parameter to enable CDR reference clock output. `o_cdr_divclk = refclk/N` Refer to the Required Clock Frequencies on page 26 for exact values.
CPRI PMA Options			
PMA Reference Frequency	• 153.6 MHz • 184.32 MHz • 122.88 MHz	184.32 MHz	Reference clock frequency support: • For CPRI line rates that include 8b/10b soft PCS, use a reference clock of 153.6 MHz or 122.88 MHz. • For CPRI line rates that include 64b/66b hard PCS, use a reference clock of 184.32 MHz or 122.88 MHz.
Configuration, Debug, and Extension Option			
Enable Debug Endpoint for Datapath and PMA Avalon Memory-Mapped Interface	• On • Off	Off	When turned **On**, the F-Tile CPRI PHY Intel FPGA IP core includes an embedded Debug Endpoint that internally connects the Avalon memory-mapped agent interface. The Debug Endpoint can access the reconfiguration space of the Datapath and PMA interface block. it can perform certain tests and debug functions through JTAG using the System Console. This option may require that you include a `jtag_debug` link in the system.

For parameters in the **Example Design** tab, refer to the device specific *F-Tile CPRI PHY Intel FPGA IP Design Example User Guide*.

For parameters in the **Analog Parameters** tab, refer to the *F-tile Architecture and PMA and FEC Direct PHY IP User Guide*.

When the CPRI rate is 6.1440G and below, there are extra 3 analog parameters to configure:

- RXEQ VGA Gain
- RXEQ High Frequency Boost
- RXEQ DFE Data Tap1

Figure 6. For CPRI Rates 9.8304G and Above

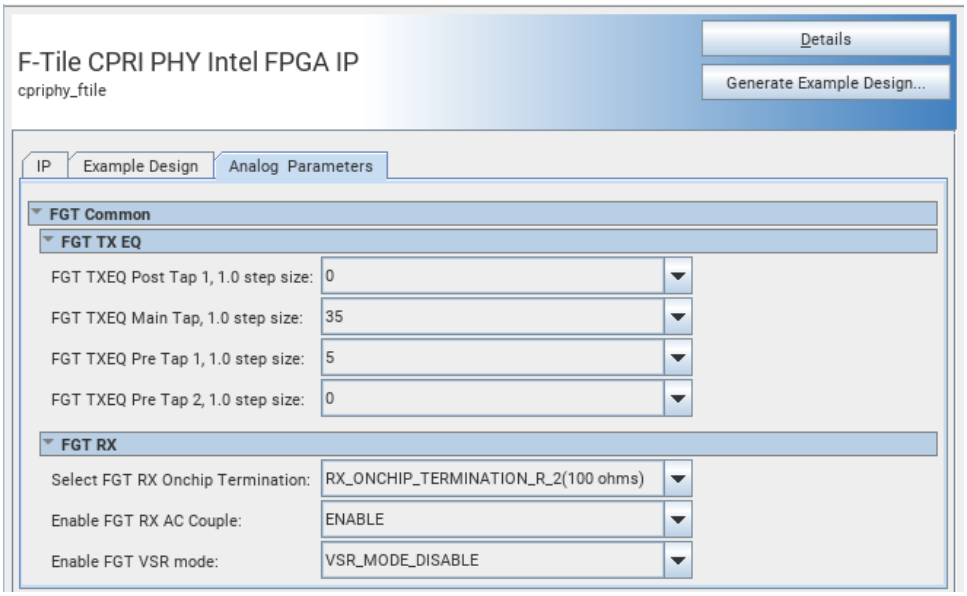
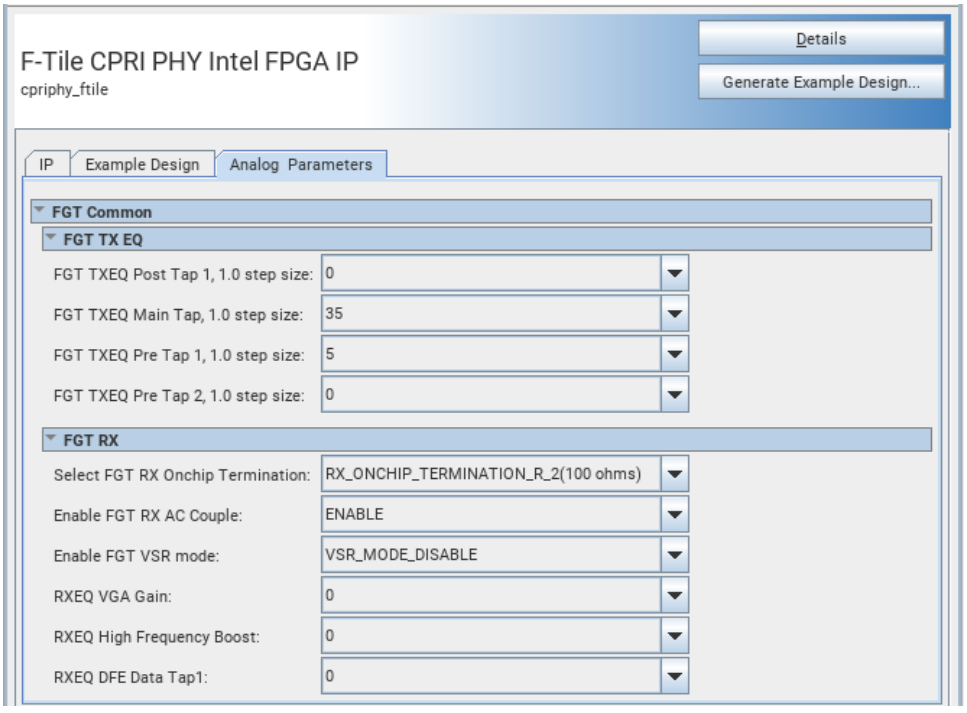


Figure 7. For CPRI Rates 6.1440G and Below



The default and recommended analog parameters values are shown in the table below:

Table 9. Default and Recommended Analog Parameter Values

Parameter	Value
FGT TXEQ Post Tap 1, 1.0 step size	0
FGT TXEQ Main Tap 1.0 step size	35
FGT TXEQ Pre Tap 1, 1.0 step size	5
FGT TXEQ Pre Tap 2, 1.0 step size	0
FGT RX Onchip Termination	RX_ONCHIP_TERMINATION_R_2 (100 ohms)
Enable FGT RX AC Couple	ENABLE
Enable FGT VSR mode	• VSR_MODE_LOW_LOSS (for CPRI rate 24Gbps only) • VSR_MODE_DISABLE (shown error if it's not selected for CPRI rate below 24Gbps)
RXEQ VGA Gain	0 (Required only when CPRI rate is 6.1440Gbps and below)
RXEQ High Frequency Boost	0 (Required only when CPRI rate is 6.1440Gbps and below)
RXEQ DFE Data Tap1	0 (Required only when CPRI rate is 6.1440Gbps and below)

In the Example Design tab, if you select Target Development Kit to be Intel Agilex 7 FPGA I-Series Transceiver-SoC Development Kit, and you configure analog parameters other than the default and recommended values, you will see warnings to recommend you set to the default values.

Figure 8. Target Development Kit in the Example Design Tab

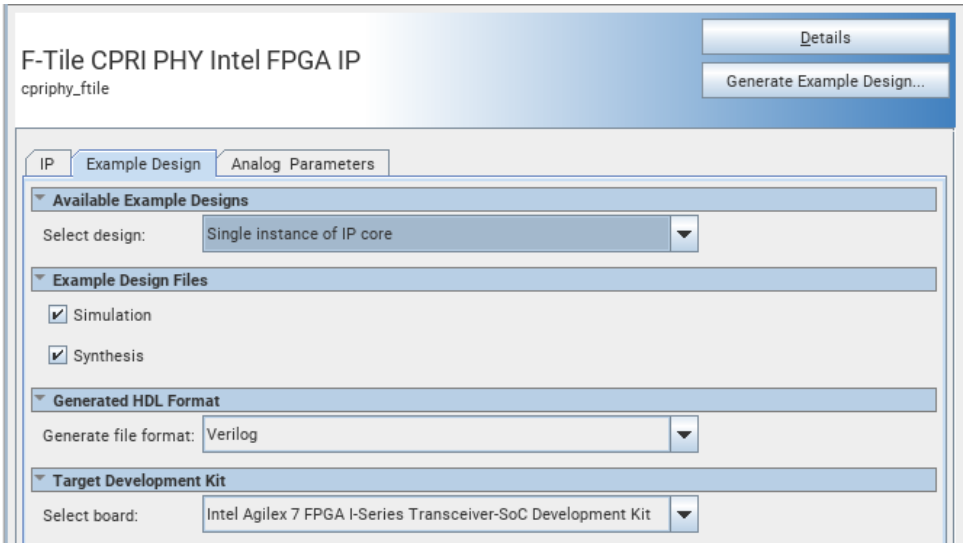
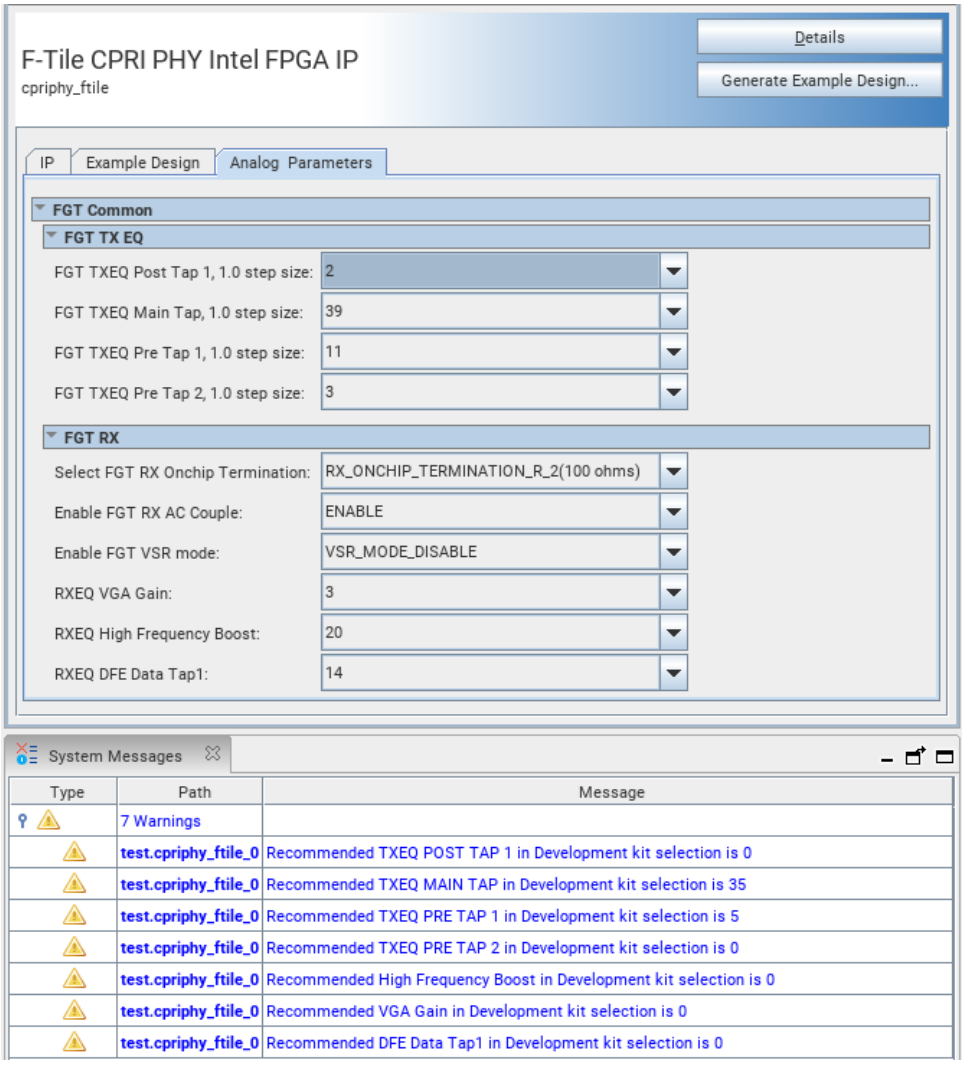


Figure 9. Warnings



Related Information

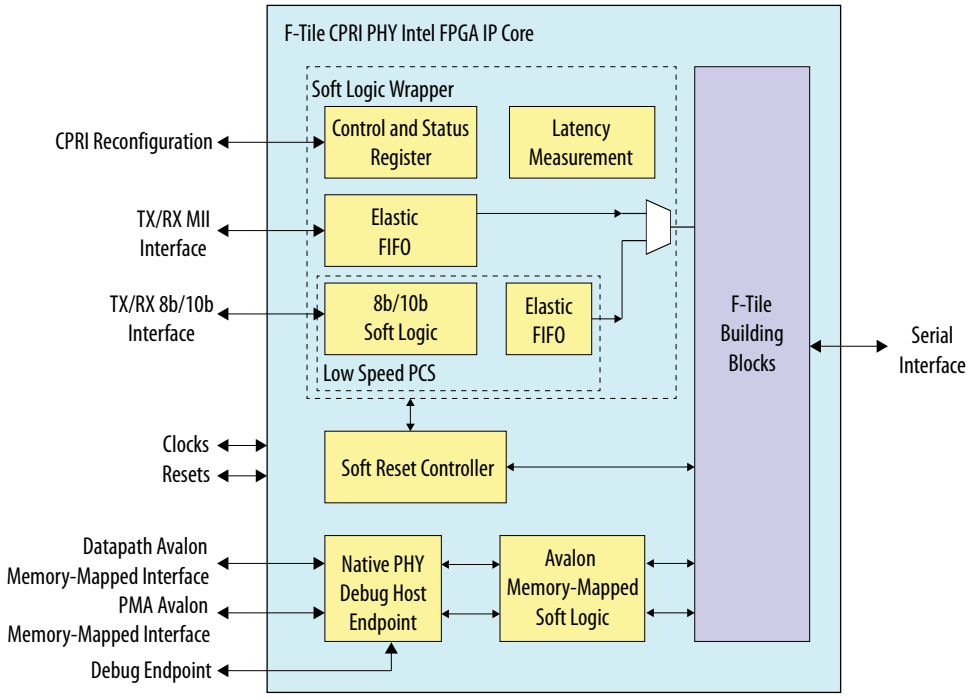
F-Tile CPRI PHY Intel FPGA IP Design Example User Guide

4. Functional Description

The F-Tile CPRI PHY Intel FPGA IP core consists of the following modules:

- F-Tile transceiver channels which consists of PMA and RS-FEC hard logic to support CPRI and Ethernet protocols. It also contains a hard PCS block that provides 64b/66b encoding scheme for 10.1376, 12.1651, and 24.33024 Gbps CPRI line rates. For more information, refer to the *F-tile Architecture and PMA and FEC Direct PHY IP User Guide*.
- Soft Reset Controller—a reset controller that manages reset signals according to the F-Tile CPRI PHY Intel FPGA IP core requirements.
- Elastic FIFO (EFIFO)—a dual clock FIFO that matches the rate differences between the F-tile hard logic and soft logic.
- Latency measurement—a module that generates a sync pulse to measure the datapath delay of the F-Tile CPRI PHY Intel FPGA IP core.
- Low Speed PCS—a soft PCS block that provides the 8b/10b encoding scheme for the CPRI line rates of 9.8 Gbps and below.

Figure 10. IP Block Diagram



Related Information

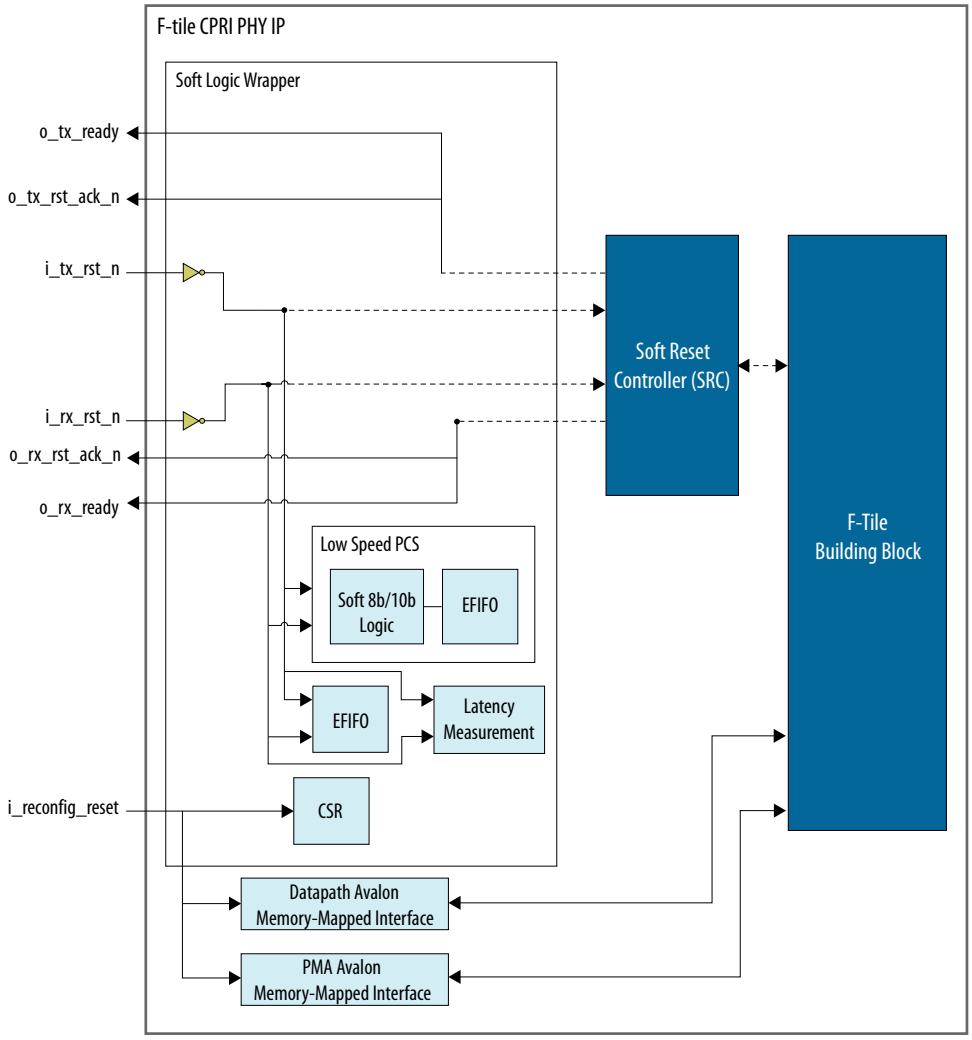
F-tile Architecture and PMA and FEC Direct PHY IP User Guide

4.1. Reset Logic

There are three main user accessible reset ports:

- `i_tx_rst_n`—resets the TX datapath.
- `i_rx_rst_n`—resets the RX datapath.
- `i_reconfig_reset`—resets the Avalon memory-mapped interface connections to PCS + PMA CSRs, and soft IP CSR.

Figure 11. Reset Block Diagram



4.2. Latency Measurement

The latency measurement in the F-Tile CPRI PHY Intel FPGA IP core measures the delay between the FPGA core and the serial pins.

4.2.1. Deterministic Latency

Deterministic Latency (DL) is the ability to precisely determine the delay between the FPGA core and the PMA pins. Such delay varies from reset to reset and device to device. In most applications, the variability is acceptable to determine the actual delay within a given reset session. This section provides an example that shows the calculation delay between pins and FPGA core for the F-Tile CPRI PHY Intel FPGA IP core.

The deterministic latency measurement methodology for Intel Agilex 7 F-tile devices derives from measuring the time when a given word is present the interface to the PMA, and when that same word arrives at the FPGA core. The difference in time between these two events, when added to the PMA propagation delay, determines the total latency between the FPGA core and the serial pins. Such a calculation intrinsically includes all delays due to intermediate logic, FIFOs, and all other effects.

Table 10. Deterministic Latency Factors

Factor	Description
`TxDL`	Transmitter delay in sampling clock cycle. To calculate the TxDL value, read the CPRI PHY register 0xC bit[20:0]. The register provides the value in fixed point format. Bit[20:8] represents an integer, and bit[7:0] represents a fractional number. For example: • Bit[20:8] = 0x27, the integer value is 39. • Bit[7:0] = 0xF4, the fractional value is 0.953125. Therefore, the total delay is 39.953125 clock cycles. *Note:* These values are available in simulation output.
`RxDL`	Receiver delay in sampling clock cycle. To calculate the RxDL value, read the CPRI PHY register 0x10 bit [20:0]. The register provides a value in fixed point format. Bit[20:8] represents an integer, and bit[7:0] represents a fractional number. For example: • Bit[20:8] = 0x27, the integer value is 39. • Bit[7:0] = 0xF4, the fractional value is 0.953125. Therefore, the total delay is 39.953125 clock cycles. *Note:* These values are available in simulation output.
`sampling_clock_period`	For F-Tile CPRI PHY Intel FPGA IP core: • Sampling clock is 250 MHz. • Period is 4 ns.
`wa`	Word Aligner bit slip value (5 bit) obtained from F-tile CPRI PHY register 0x4[9:5].
`eth_wa`	Word Aligner bit slip value (7 bit) obtained from the Datapath Avalon Memory-Mapped Interface register 0x1110[6:0].
`ethlphy_wa`	RS-FEC Word Aligner bit slip value (lowest 5 bit) obtained from the Datapath Avalon Memory-Mapped Interface register 0x6174[4:0].
`dlpulse`	Obtained from the Datapath Avalon Memory-Mapped Interface register (pcs_bitslip_cnt) at 0x1110 [7].

Table 11. System Clock Frequency and Period

System Clock Frequency	system_clk_div2 period
805.664062 MHz	2.482424 ns
830.078125 MHz	2.409412 ns
903.125000 MHz	2.214533 ns

Table 12. Delay Equations for 1.2G/2.4G/3G/4.9G/6G/9.8G Variants

Delay Equations		For 1.2G/2.4G/3G/4.9G/6G/9.8G Variants
Regular Simulation	TX Delay (ns)	`TxDL * 4ns + 6 * system_clk_div2 period + 229 * UI`
	RX Delay (ns)	`RxDL * 4ns - 6 * system_clk_div2 period + (347.5 + wa) * UI`
FastSim(1)	TX Delay (ns)	`TxDL * 4ns + 6 * system_clk_div2 period + 199.5 * UI`
	RX Delay (ns)	`RxDL * 4ns - 6 * system_clk_div2 period + (339.5 + wa) * UI`

Table 13. Delay Equations for 10G/12G/24G with RS-FEC Variants

Delay Equations		For 10G/12G/24G with RS-FEC Variants
Regular Simulation	TX Delay (ns)	`TxDL * 4ns + 6 * system_clk_div2 period + 211 * UI`
	RX Delay (ns)	`RxDL * 4ns - 6 * system_clk_div2 period + (53.5 - ethlphy_wa) * UI`
FastSim(1)	TX Delay (ns)	`TxDL* 4ns + 6 * system_clk_div2 period + 162.5 * UI`
	RX Delay (ns)	`RxDL * 4ns - 6 * system_clk_div2 period + (61.5 - ethlphy_wa) * UI`

Table 14. Delay Equations for 10G/12G/24G without RS-FEC Variants

Delay Equations		For 10G/12G/24G without RS-FEC Variants
Regular Simulation	TX Delay (ns)	`TxDL * 4ns + 6 * system_clk_div2 period + 211 * UI`
	RX Delay (ns)	`RxDL * 4ns - 6 * system_clk_div2 period + (53.5 - eth_wa - 33 * dlpulse) * UI`
FastSim(1)	TX Delay (ns)	`TxDL * 4ns + 6 * system_clk_div2 period + 162.5 * UI`
	RX Delay (ns)	`RxDL * 4ns - 6 * system_clk_div2 period + (61.5 - eth_wa - 33 * dlpulse) * UI`

Table 15. Delay Equations for 2.4G/4.9G/9.8G/10G Tunnel Mode

Delay Equations		For 10G/12G/24G without RS-FEC Variants
Regular Simulation	TX Delay (ns)	`tx_delay * 4ns + 6 * system_clk_div2 period + 143 * UI`
	RX Delay (ns)	`rx_delay * 4ns - 6 * system_clk_div2 period + (184+wa) * UI`
FastSim(1)	TX Delay (ns)	`tx_delay * 4ns + 6 * system_clk_div2 period + 96.5 * UI`
	RX Delay (ns)	`rx_delay * 4ns - 6 * system_clk_div2 period + (191.5+wa) * UI`

(1) This simulation model is not supported by the Questa Intel FPGA Edition simulator.

To enable the FAST_SIM option, set the following value in your simulation script:

```
set FAST_SIM_OPTIONS "+define+IP7581SERDES_UX_SIMSPEED"
```

To disable the FAST_SIM option, set the following value in your simulation script:

```
set FAST_SIM_OPTIONS ""
```

4.2.2. Calculation for 64b/66b Datapath

If the 64b/66b datapath RSFEC is enabled, perform the following steps to configure the DL logic in F-tile before the RX latency calculation:

1. Ensure the `o_rx_blocklock` signal is asserted.
2. Read the RSFEC code word position value from `rsfec_cw_pos_rx` register, `num` field using the Datapath Avalon memory-mapped interface. For more information, refer to the F-Tile Ethernet Intel FPGA Hard IP Register Map.
3. Program the RSFEC code word position value to FGT `fgt_q_dl_ctrl_a_l<x>` register, `cfg_rx_lat_bit_for_async` field using the PMA Avalon memory-mapped interface. The `fgt_q_dl_ctrl_a_l<x>` register is based on the placement of the FGT transceiver:
   a. FGT15, FGT11, FGT7, FGT3: fgt_q_dl_ctrl_a_l3
   b. FGT14, FGT10, FGT6, FGT2: fgt_q_dl_ctrl_a_l2
   c. FGT13, FGT9, FGT5, FGT1: fgt_q_dl_ctrl_a_l1
   d. FGT12, FGT8, FGT4, FGT0: fgt_q_dl_ctrl_a_l0

   For more information, refer to the F-Tile PMA/FEC Direct PHY Intel FPGA IP Register Map.
4. Reset the deterministic measure logic for RX datapath by asserting the `rx_dl_restart` bit at register offset 0x8 using the `reconfig_cpri` interface.
5. Release the reset for deterministic measure logic for RX datapath by clearing the `rx_dl_restart` bit at register offset 0x8 using the `reconfig_cpri` interface.

5. Interface Signals

5.1. Clock Signals

Each CPRI PHY channel has its own pair of datapath clocks and each transceiver has its own reference clock. The reconfiguration clock is shared.

Table 16. CPRI PHY Clock Input Signals

Port name	Width (Bits)	Description
system_pll_clk_link	1	System PLL clock link port.
tx_pll_refclk_link	1	TX PLL reference clock link port.
rx_cdr_refclk_link	1	RX CDR reference clock link port.
i_reconfig_clk	1	Reconfiguration clock.
i_sampling_clk	1	Sampling clock for deterministic latency logic.

Table 17. Clock Source Signals

This table lists the clock source ports for the CPRI core. The IP core provides locally generated PLL clocks and recovered clocks that can be used for the datapath.

Signal Name	Width (Bits)	I/O Direction	Description
o_tx_clkout	1	Output	System clock divided by 2.
o_tx_clkout2	1	Output	Parallel TX clock: • For 64B/66B PCS, running at line rate/66. • For 8B/10B PCS, running at line rate/20. Hold circuits using this clock in reset until o_tx_pll_lock is high.
o_rx_clkout	1	Output	System clock divided by 2.
o_rx_clkout2	1	Output	Parallel RX recovered clock: • For 64B/66B PCS, running at line rate/66. • For 8B/10B PCS, running at line rate/20. Hold circuits using this clock in reset until o_rx_cdr_lock is high.

Table 18. Clock Status Signals

This table lists the clock status ports for the CPRI core. Use these ports to hold the circuits that use clock sources from the IP core in reset until the PLLs driving the clocks are locked.

Signal Name	Width (Bits)	I/O Direction	Description
o_tx_pll_lock	1	Output	Indicates the TX PLL driving clock signals from the core is locked. Do not use the o_tx_clkout or o_tx_clkout2 clocks until the o_tx_pll_lock clock is high.
o_rx_cdr_lock	1	Output	Indicates that the recovered clocks are locked to data. Do not use the o_rx_clkout or o_rx_clkout2 clocks until the o_rx_cdr_lock clock is high.

5.1.1. Required Clock Frequencies

Table 19. Required Clock Frequencies

Port Name	Frequency (MHz)	Notes
i_reconfig_clk	100	Provides CSR access on all the Avalon memory-mapped interfaces.
o_tx_clkout	402.83203125 415.0390625 451.5625	System clock divided by 2.
o_tx_clkout2	368.64	CPRI PHY system clock times (64/66) for 24G channels.
	184.32	CPRI PHY system clock times (64/66) for 12G channels.
	153.6	CPRI PHY system clock times (64/66) for 10G channels.
	491.52	CPRI PHY system clock for 9.8G channels.
	307.2	CPRI PHY system clock for 6G channels.
	245.76	CPRI PHY system clock for 4.9G channels.
	153.6	CPRI PHY system clock for 3G channels.
	122.88	CPRI PHY system clock for 2.4G channels.
	61.44	CPRI PHY system clock for 1.2G channels.
o_rx_clkout	402.83203125 415.0390625 451.5625	System clock divided by 2
o_rx_clkout2	368.64	Derived from recovered clock for 24G channels.
	184.32	Derived from recovered clock for 12G channels.
	153.6	Derived from recovered clock for 10G channels.
	491.52	Derived from recovered clock for 9.8G channels.
	307.2	Derived from recovered clock for 6G channels.
	245.76	Derived from recovered clock for 4.9G channels.
	153.6	Derived from recovered clock for 3G channels.
	122.88	Derived from recovered clock for 2.4G channels.
	61.44	Derived from recovered clock for 1.2G channels.

continued...

Port Name	Frequency (MHz)	Notes	
i_sampling_clk	250	Sampling clock for deterministic logic from external source.	
o_cdr_divclk	92.16	refclk = 184.32 MHz	Derived from reference clock for 24G channels (refclk/N, N=2).
	30.72		Derived from reference clock for 12G channels (refclk/N, N=6).
	30.72		Derived from reference clock for 10G channels (refclk/N, N=6).
	25.6	refclk = 153.6 MHz	Derived from reference clock for 9.8G channels (refclk/N, N=6).
	25.6		Derived from reference clock for 6G channels (refclk/N, N=6).
	25.6		Derived from reference clock for 4.9G channels (refclk/N, N=6).
	25.6		Derived from reference clock for 3G channels (refclk/N, N=6).
	25.6		Derived from reference clock for 2.4G channels (refclk/N, N=6).
	25.6		Derived from reference clock for 1.2G channels (refclk/N, N=6).
	61.44	refclk = 122.88 MHz	Derived from reference clock for 24G channels (refclk/N, N=2).
	61.44		Derived from reference clock for 12G channels (refclk/N, N=2).
	30.72		Derived from reference clock for 10G channels (refclk/N, N=4).
	61.44		Derived from reference clock for 9.8G channels (refclk/N, N=2).
	61.44		Derived from reference clock for 6G channels (refclk/N, N=2).
	61.44		Derived from reference clock for 4.9G channels (refclk/N, N=2).
	61.44		Derived from reference clock for 3G channels (refclk/N, N=2).
	61.44		Derived from reference clock for 2.4G channels (refclk/N, N=2).
	61.44		Derived from reference clock for 1.2G channels (refclk/N, N=2).

5.2. Reset Signals

Each of the CPRI PHY Channels in the core has its own set of reset signals. The i_reconfig_reset port is shared.

Table 20. Reset Signals

Port Name	Width (Bits)	Domain	Description
i_tx_rst_n	1	Asynchronous	Resets the selected TX datapath. Active low.
o_tx_rst_ack_n	1	Asynchronous	TX datapath reset acknowledgement. Active low.
o_tx_ready	1	Asynchronous	TX datapath is out of reset and ready.
i_rx_rst_n	1	Asynchronous	Resets the selected RX datapath. Active low.
o_rx_rst_ack_n	1	Asynchronous	RX datapath reset acknowledgement. Active low.
o_rx_ready	1	Asynchronous	RX datapath is out of reset and ready.
i_reconfig_reset	1	i_reconfig_clk	Reconfig reset. Resets the Avalon memory-mapped interface connections to the F-tile and resets Soft CSR. It does not reset F-tile CSRs. Active high. Must be asserted once upon power-up.

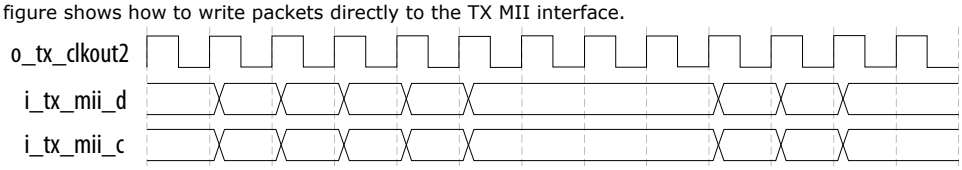
5.3. TX MII Interface (64b/66b)

Table 21. TX MII Interface

Port Name	Width (Bits)	Domain	Description
i_tx_mii_d[63:0]	64	o_tx_clkout2	TX MII data. Data must be in MII encoding. i_tx_mii_d[7:0] holds the first byte that the IP core transmits on the CPRI link. i_tx_mii_d[0] holds the first bit the IP core transmits on the CPRI link.
i_tx_mii_c[7:0]	8	o_tx_clkout2	TX MII control bits. Each bit corresponds to a byte of the TX MII data signal. For example, i_tx_mii_c[0] corresponds to i_tx_mii_d[7:0], i_tx_mii_c[1] corresponds to i_tx_mii_d[15:8], and so on. If the value of a bit is 1, the corresponding data byte is a control byte. If the value of a bit is 0, the corresponding data byte is data. The Start of Packet byte (0xFB) and End of Packet byte (0xFD) are control bytes.

Figure 12. Transmitting Data Using TX MII Interface

This figure shows how to write packets directly to the TX MII interface.



- The packets are written using MII. Each byte in i_tx_mii_d has a corresponding bit in i_tx_mii_c that indicates whether the byte is a control byte or a data byte; for example, i_tx_mii_c[1] is the control bit for i_tx_mii_d[15:8].
- The byte order for the TX MII interface flows from right to left; the first byte to be transmitted from the interface is i_tx_mii_d[7:0].
- The first bit to be transmitted from the interface is i_tx_mii_d[0].

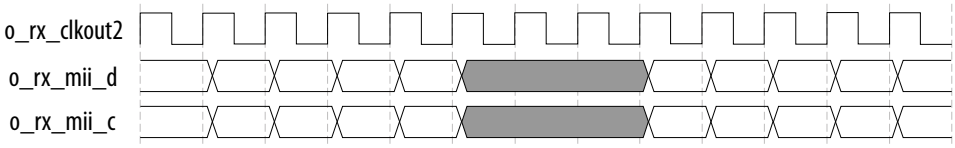
5.4. RX MII Interface (64b/66b)

Table 22. RX MII Interface

Port Name	Width (Bits)	Domain	Description
o_rx_mii_d[63:0]	64	o_rx_clkout2	RX MII data. Data is in MII encoding. o_rx_mii_d[7:0] holds the first byte that the IP core received on the CPRI link. o_rx_mii_d[0] holds the first bit that the IP core received on the CPRI link.
o_rx_mii_c[7:0]	8	o_rx_clkout2	RX MII control bits. Each bit corresponds to a byte of RX MII data. o_rx_mii_c[0] corresponds to o_rx_mii_d[7:0], o_rx_mii_c[1] corresponds to o_rx_mii_d[15:8], and so on. If the value of a bit is 1, the corresponding data byte is a control byte. If the value of a bit is 0, the corresponding data byte is data. The Start of Packet byte (0xFB) and End of Packet byte (0xFD) are control bytes.

Figure 13. Receiving Data Using the RX MII Interface

This figure shows how to read packets from the RX MII interface.



- The packets are MII encoded. Each byte in o_rx_mii_d has a corresponding bit in o_rx_mii_c that indicates whether the byte is a control byte or a data byte; for example, o_rx_mii_c[2] is the control bit for o_rx_mii_d[23:16].
- The byte order for the RX MII interface flows from right to left. The first byte that the core receives is o_rx_mii_d[7:0].
- The first bit that the IP receives is o_rx_mii_d[0].

5.5. Status Interface for 64b/66b Line Rate

This section lists the status ports for the CPRI PHY 64b/66b line rate. Each CPRI PHY channel has its own status port.

Table 23. Status Interface Signals for 64b/66b Interface

Port Name	Width (Bits)	Domain	Description
o_rx_pcs_ready	1	Asynchronous	The IP core asserts this signal to indicate that the corresponding RX datapath is ready to receive data. The signal deasserts when i_rx_rst_n is deasserted.
o_rx_block_lock	1	Asynchronous	The IP core asserts this signal to indicate that 66b block alignment has completed for the corresponding CPRI PHY channel.
o_rx_hi_ber	1	Asynchronous	The IP core asserts this signal in accordance with IEEE 802.3 to indicate RX PCS is in Hi-Bit Error Rate (BER) state for the corresponding CPRI PHY channel.
o_tx_hip_ready	1	Asynchronous	The IP core asserts this signal after i_tx_rst_n is asserted to indicate that the CPRI PHY has completed all internal initialization, is ready to accept reconfiguration transactions and send data.

5.6. TX Interface (8b/10b)

The TX 8b/10b interface is available only if you enable the **Enable reconfiguration to 8b/10b datapath** parameter or if you select the 8b/10b CPRI line rate. For the CPRI PHY core to power up in the 64b/66b line rate, the IP core asserts these signals when you reconfigure the core at runtime to enter the 8b/10b line rate.

Table 24. TX 8b/10b Interface

Port Name	Width (Bits)	Domain	Description
i_tx_d[15:0]	16	o_tx_clkout2	Indicates 8b/10b TX data for the corresponding CPRI PHY channel.
i_tx_c[1:0]	2	o_tx_clkout2	Indicates 8b/10b TX control for the corresponding CPRI PHY channel.

When you transmit the data using the TX 8b/10b interface:

- The frames are 8b/10b encoded. Each byte in i_tx_d has a corresponding bit in i_tx_c that indicates whether the byte is a control byte or a data byte. For example, i_tx_c[1] is the control bit for i_tx_d[15:8].
- The byte order for the TX interface flows from right to left and the first byte that the core transmits is i_tx_d[7:0].
- The first bit that the core transmits is i_tx_d[0].

5.7. RX Interface (8b/10b)

The RX 8b/10b interface is available only if you enable the **Enable reconfiguration to 8b/10b datapath** parameter or if you select the 8b/10b CPRI line rate. For the CPRI PHY core to power up in the 64b/66b line rate, the IP core asserts these signals when you reconfigure the core at runtime to enter the 8b/10b line rate.

Table 25. RX 8b/10b Interface

Port Name	Width (Bits)	Domain	Description
i_rx_d[15:0]	16	o_rx_clkout2	Indicates 8b/10b RX data for the corresponding CPRI PHY channel.
i_rx_c[1:0]	2	o_rx_clkout2	Indicates 8b/10b RX control for the corresponding CPRI PHY channel.

When you transmit the data using the RX 8b/10b interface:

- The frames are 8b/10b encoded. Each byte in i_rx_d has a corresponding bit in i_rx_c that indicates whether the byte is a control byte or a data byte. For example, i_rx_c[0] is the control bit for i_rx_d[7:0].
- The byte order for the RX interface flows from right to left and the first byte that the core receives is i_rx_d[7:0].
- The first bit that the core receives is i_rx_d[0].

5.8. Status Interface for 8b/10b Line Rate

This section lists the status ports for the CPRI PHY 8b/10b line rate. Each CPRI PHY channel has its own status port.

Table 26. CPRI PHY Status Interface Signals for 8b/10b Interface

Port Name	Width (Bits)	Domain	Description
o_rx_patterndetect	1	o_rx_clkout2	The IP core asserts this signal to indicate that K28.5 has been detected in the current word boundary of o_rx_d or o_rx_c and the received data from the RX PMA achieved the word alignment. This interface should be observed in conjunction with o_rx_disperr and i_rx_errdetect.
o_rx_disperr[1:0]	2	o_rx_clkout2	The IP core asserts this signal to indicate that the IP received 10-bit code or data group in the current word boundary of o_rx_d or o_rx_c has a disparity error. • Bit 0: Indicates status for lower data group. • Bit 1: Indicates status for higher data group.
o_rx_errdetect[1:0]	2	o_rx_clkout2	The IP core asserts this signal to indicate that it received 10-bit data group in the o_rx_d or o_rx_c has an 8b/10b code violation. • Bit 0: Indicates status for lower data group. • Bit 1: Indicates status for higher data group.

5.9. Serial Interface

The CPRI PHY IP core always includes the serial ports.

Table 27. Serial Interface

Port Name	Width	Description
o_tx_serial	1	TX serial data for the corresponding F-tile CPRI PHY channel.
o_tx_serial_n	1	TX serial data *(n)* for the corresponding F-tile CPRI PHY channel.
i_rx_serial	1	RX serial data for the corresponding F-tile CPRI PHY channel.
i_rx_serial_n	1	RX serial data *(n)* for the corresponding F-tile CPRI PHY channel.

5.10. CPRI PHY Reconfiguration Interface

Table 28. CPRI PHY Reconfiguration Interface

Port Name	Width (Bits)	Domain	Description
i_reconfig_cpri_addr[3:0]	4	i_reconfig_clk	Address for F-tile CPRI PHY CSRs in the selected channel. Using word addressing format.
i_reconfig_cpri_read	1	i_reconfig_clk	Read command for F-tile CPRI PHY CSRs in the selected channel.
i_reconfig_cpri_write	1	i_reconfig_clk	Write command for F-tile CPRI PHY CSRs in the selected channel.
o_reconfig_cpri_readdata[31:0]	32	i_reconfig_clk	Read data from reads to F-tile CPRI PHY CSRs in the selected channel.
o_reconfig_cpri_readdatavalid	1	i_reconfig_clk	Read data from F-tile CPRI PHY CSRs is valid in the selected channel.
i_reconfig_cpri_writedata[31:0]	32	i_reconfig_clk	Data for writes to F-tile CPRI PHY CSRs in the selected channel.
o_reconfig_cpri_waitrequest	1	i_reconfig_clk	Avalon memory-mapped interface stalling signal for operations on F-tile CPRI PHY CSRs in the selected channel.

Figure 14. Writing to CPRI PHY Reconfiguration

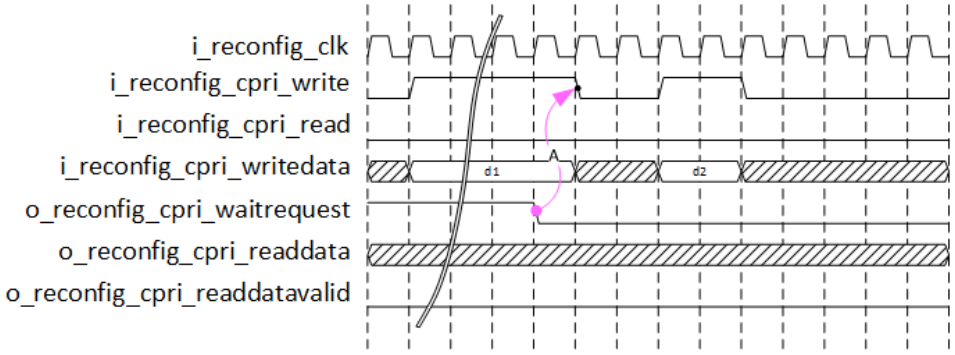
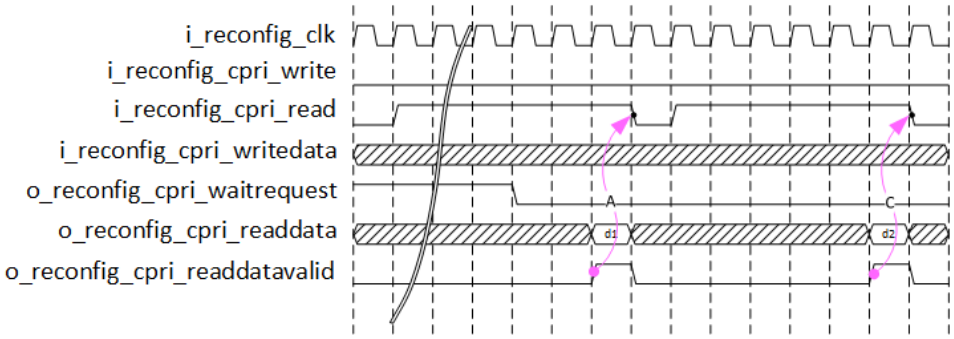


Figure 15. Reading from CPRI PHY Reconfiguration



5.11. Datapath Avalon Memory-Mapped Interface

Table 29. Datapath Avalon Memory-Mapped Interface Signals

Port Name	Width (Bits)	Domain	Description
i_reconfig_eth_addr[13:0]	14	i_reconfig_clk	Address for the Datapath Avalon Memory-Mapped Interface CSRs in the selected channel. Using word addressing format.
i_reconfig_eth_read	1	i_reconfig_clk	Read command for the Datapath Avalon Memory-Mapped Interface CSRs in the selected channel.
i_reconfig_eth_write	1	i_reconfig_clk	Write command for the Datapath Avalon Memory-Mapped Interface CSRs in the selected channel.
o_reconfig_eth_readdata[31:0]	32	i_reconfig_clk	Read data from reads to the Datapath Avalon Memory-Mapped Interface CSRs in the selected channel.
o_reconfig_eth_readdatavalid	1	i_reconfig_clk	Read data from the Datapath Avalon Memory-Mapped Interface CSRs is valid in the selected channel.
i_reconfig_eth_writedata[31:0]	32	i_reconfig_clk	Data for writes to the Datapath Avalon Memory-Mapped Interface CSRs in the selected channel.
o_reconfig_eth_waitrequest	1	i_reconfig_clk	Avalon memory-mapped interface stalling signal for operations on the Datapath Avalon Memory-Mapped Interface CSRs in the selected channel.
i_reconfig_eth_byteenable[3:0]	4	i_reconfig_clk	Byte-enable for the Datapath Avalon Memory-Mapped Interface CSRs in the selected channel.

5.12. PMA Avalon Memory-Mapped Interface

Table 30. PMA Avalon Memory-Mapped Interface Signals

Port Name	Width	Domain	Description
i_reconfig_xcvr_addr[17:0]	18	i_reconfig_clk	Address for the PMA Avalon Memory-Mapped Interface CSRs in the selected channel. Using word addressing format.
i_reconfig_xcvr_read	1	i_reconfig_clk	Read command for the PMA Avalon Memory-Mapped Interface CSRs in selected the channel.
i_reconfig_xcvr_write	1	i_reconfig_clk	Write command for the PMA Avalon Memory-Mapped Interface CSRs in the selected channel.
o_reconfig_xcvr_readdata[31:0]	32	i_reconfig_clk	Read data from reads to the PMA Avalon Memory-Mapped Interface CSRs in the selected channel.
o_reconfig_xcvr_readdatavalid	1	i_reconfig_clk	Read data from the PMA Avalon Memory-Mapped Interface CSRs is valid in the selected channel.
i_reconfig_xcvr_writedata[31:0]	32	i_reconfig_clk	Data for writes to the PMA Avalon Memory-Mapped Interface CSRs in the selected channel.
o_reconfig_xcvr_waitrequest	1	i_reconfig_clk	Avalon memory-mapped interface stalling signal for operations on the PMA Avalon Memory-Mapped Interface CSRs in the selected channel.
i_reconfig_xcvr_byteenable[3:0]	4	i_reconfig_clk	Byte-enable for the PMA Avalon Memory-Mapped Interface CSRs in the selected channel.

6. IP Registers

You can access the CPRI registers for the F-Tile CPRI PHY Intel FPGA IP core using the Avalon memory-mapped interface.

Table 31. Address Ranges

Register Type	Address Range
CPRI PHY Registers	0x0-0x3C

- F-Tile CPRI PHY Intel FPGA IP Register Map

Related Information

F-Tile PMA and FEC Direct PHY Intel FPGA IP Register Map

7. F-Tile CPRI PHY Intel FPGA IP User Guide Archives

For the latest and previous versions of this user guide, refer to the F-Tile CPRI PHY Intel FPGA IP User Guide HTML version. Select the version and click **Download**. If an IP or software version is not listed, the user guide for the previous IP or software version applies.

8. Document Revision History for the F-Tile CPRI PHY Intel FPGA IP User Guide

Document Version	Intel Quartus Prime Version	IP Version	Changes
2023.10.02	23.3	4.3.0	In the IP Parameter Settings section, added the Analog Parameters information.
2023.04.03	23.1		• Updated product family name to "Intel Agilex 7."
2023.02.03	22.4	4.1.0	Deterministic Latency on page 22: Instances of signal `ethlphy_wa` changed to `eth_wa` occurring in the table *Delay Equations for 10G/12G/24G without RS-FEC Variants*
2022.09.26	22.3	4.0.0	• Added support for new reference clock (122.88 MHz). — Updated the following sections: • *Supported Features* • *IP Parameter Settings* • *Required Clock Frequencies* • Corrected register names in section: *Calculation for 64b/66b Datapath*.
2022.06.21	22.2	3.3.0	Added the hardware design example support for: • Intel Agilex I-Series FPGA Development Kit • Intel Agilex I-Series Transceiver-SoC Development Kit
2022.03.28	22.1	3.2.0	• Removed support for ModelSim* SE simulator. • Added a new parameter: **Enable CDR Clock Output**. • Updated the *Required Clock Frequencies* section.

continued...

Document Version	Intel Quartus Prime Version	IP Version	Changes
2021.12.13	21.4	3.1.0	• Added support for Xcelium simulator. • Updated the *Resource Utilization*. • Added a new parameter: **Enable Debug Endpoint for Datapath and PMA Avalon Memory-Mapped Interface**.
2021.10.04	21.3	3.0.0	• Added support for the following line rates: — 1.228 Gbps — 3.072 Gbps — 6.144 Gbps • Updated the following sections with new line rate information: — *Supported Features* — *Resource Utilization* — *IP Parameter Settings* • Updated the deterministic latency equations in section: *Deterministic Latency*. • Updated the address range for the *IP Registers*. • Added support for the following simulators: — Siemens EDA QuestaSim simulator — Questa Intel FPGA Edition simulator
2021.06.21	21.2	2.0.0	Initial release.